REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, change I_{CCT}. Change table I footnotes. Change figure 3.	88-11-17	Mike A. Frye
B	Add group C to 4.2.a(1) and 4.3.a(1). Editorial changes throughout.	90-07-13	Don Cool
C	Inactivate device 02. Table I, correct I_{CCQ}, I_{CCT}. Add devices 03 and 04. Editorial changes throughout.	92-06-22	Tim Noh

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV	C	C	C	C															
SHEET	15	16	17	18															

REV STATUS OF SHEETS															
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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Michael A. Frye

DRAWING APPROVAL DATE
88-04-20

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL CMOS, HIGH PERFORMANCE PARITY BUS TRANSCEIVERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88573

SHEET 1 OF 18

DESC FORM 193
JUL 91

5962-E491

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29C853	High performance CMOS parity bus transceiver
02 1/	29C855	High performance CMOS parity bus transceiver
03	29C853A	High performance CMOS parity bus transceiver with latch option
04	29C833A	High performance CMOS parity bus transceiver

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases K, L, and 3	See MIL-M-38510, appendix C
Junction temperature (T_J)	150°C
DC output voltage range	-0.5 V dc to V_{CC} +0.5 V dc
DC output diode current:	
Into output	+50 mA
Out of output	-50 mA
DC input diode current:	
Into input	+20 mA
Out of input	-20 mA
DC output current per pin:	
I_{sink}:	
(Devices 01 and 02)	+48 mA (2 x I_{OL})
(Devices 03 and 04)	+100 mA (2 x I_{OL})
I_{source}:	
(Devices 01 and 02)	-30 mA (2 x I_{OH})
(Devices 03 and 04)	-100 mA (2 x I_{OH})
Total dc ground current 3/	(n x I_{OL} + m x I_{CCT}) mA
Total dc V_{CC} current 3/	(n x I_{OH} + m x I_{CCT}) mA

1/ Not available from an approved source of supply.
2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
3/ n = number of outputs, m = number of inputs

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -15.0 mA V_{IN} = V_{IH} or V_{IL}		1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24.0 mA	1, 2, 3	01, 02		0.5	V
			I_{OL} = 32 mA		03, 04			
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3	All		-1.2	V
Input low current	I_{IL1}	V_{CC} = 5.5 V Inputs only 1/	V_{IN} = 0.4 V	1, 2, 3	01, 02		-5.0	µA
	I_{IL2}		V_{IN} = 0 V		01, 02		-10.0	µA
					03, 04		-5.0	
Input high current	I_{IH1}	V_{CC} = 5.5 V Inputs only 1/	V_{IN} = 2.7 V	1, 2, 3	01, 02		5.0	µA
	I_{IH2}		V_{IN} = 5.5 V		01, 02		10.0	µA
					03, 04		5.0	
Off-state current	I_{OZH1}	V_{CC} = 5.5 V I/O port 2/	V_{OUT} = 5.5 V	1, 2, 3	01, 02		20.0	µA
					03, 04		10.00	
	I_{OZH2}		V_{OUT} = 2.7 V		01, 02		15.0	µA
Off-state current	I_{OZL1}	V_{CC} = 5.5 V I/O port 2/	V_{OUT} = 0.4 V	1, 2, 3	01, 02		-15	µA
	I_{OZL2}		V_{OUT} = 0 V		01, 02		-20	µA
					03, 04		-10	
Output short circuit current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0 V 3/		1, 2, 3	All	-60		mA
Static supply current	I_{CCQ}	V_{CC} = 5.5 V	V_{IN} = 5.5 or 0 V	1, 2, 3	01, 02		160	µA
					03, 04		1.5	mA
	I_{CCT}		V_{IN} = 3.4 V 1/		All		3.0	mA/bit
			V_{IN} = 3.4 V 2/				1.5	mA/bit

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional testing		See 4.3.1c	7, 8	All			
Input capacitance	C_{IN}	See 4.3.1.d	4	All		16	pF
Output capacitance	C_{OUT}		4			20	pF
I/O capacitance	$C_{I/O}$		4			20	pF
Propagation delay Ri to Ti, Ti to Ri	t_{PLH}	See figure 4 $R_1 = 500\Omega$ $C_L = 50$ pF $R_2 = 500\Omega$	9,10,11	01, 02		18	ns
				03, 04		12	
Propagation delay Ri to Ti, Ti to Ri	t_{PHL}		9,10,11	01, 02		18	ns
				03, 04		12	
Propagation delay Ri to parity	t_{PLH}		9,10,11	01, 02		23	ns
				03, 04		14.5	
Propagation delay Ri to parity	t_{PHL}		9,10,11	01, 02		23	ns
				03, 04		14.5	
Propagation delay EN to ERR 4/	t_{PHL}		9,10,11	01, 02		18	ns
				03, 04		14	
Propagation delay CLR to ERR	t_{PLH}		9,10,11	01, 02		23	ns
				03, 04		21	
Propagation delay Ti, parity to ERR (pass mode only)	t_{PLH}		9,10,11	01, 02		33	ns
				03		21	
Propagation delay Ti, parity to ERR (pass mode only)	t_{PHL}		9,10,11	01, 02		28	ns
				03		21	
Propagation delay OER to parity	t_{PLH}		9,10,11	01, 02		25	ns
				03, 04		15	
Propagation delay OER to parity	t_{PHL}		9,10,11	01, 02		25	ns
				03, 04		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

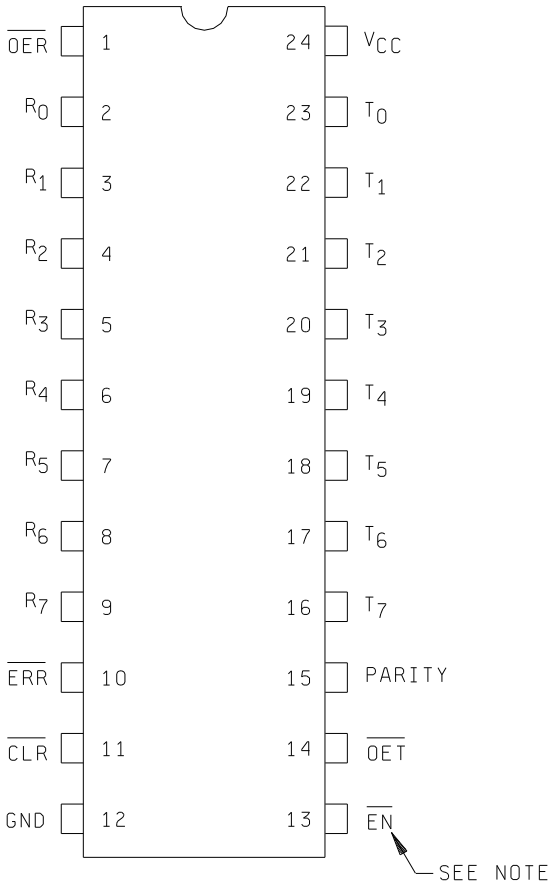
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output enable time OER, OET to Ri, Ti, and parity	t_{PZH}	See figure 4 $R_1 = 500\Omega$ $C_L = 50$ pF $R_2 = 500\Omega$	9,10,11	01, 02		18	ns
				03, 04		12	
Output enable time OER, OET to Ri, Ti, and parity	t_{PZL}		9,10,11	01, 02		18	ns
				03, 04		12	
Output disable time OER, OET to Ri, Ti, and parity	t_{PHZ}		9,10,11	01, 02		18	ns
				03, 04		12	
Output disable time OER, OET to Ri, Ti, and parity	t_{PLZ}		9,10,11	01, 02		18	ns
				03, 04		12	
Set-up time Ti, parity to EN 4/	t_S		9,10,11	01, 02	21		ns
				03, 04	10		
Hold time Ti, parity to EN 4/	t_H		9,10,11	01,02,04	2		ns
				03	3		
$\overline{EN}$ pulse width (high) 4/	t_{PWH}		9,10,11	All	9		ns
$\overline{EN}$ pulse width (low) 4/	t_{PWL}		9,10,11	All	9		ns
Clear pulse width (low)	t_{PWL}		9,10,11	All	9		ns
CLR ($\overline{CLR}$ $\neg\uparrow$) to CLK setup time	t_{REC}		9,10,11	04	4		ns

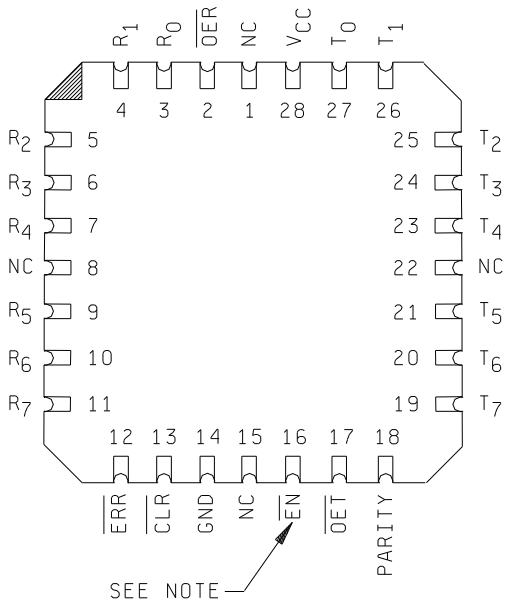
1/ Applies to $\overline{OER}$, $\overline{OET}$, $\overline{EN}$, $\overline{CLR}$.
2/ Applies to Ri, Ti, parity.
3/ Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4/ For device type 04, replace $\overline{EN}$ with CLK.

Device types 01, 02, 03, and 04

Case outlines K and L

Case outline 3





NOTE: For -04, replace $\overline{\text{EN}}$ with CLK.

FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**5962-88573**
		REVISION LEVEL C	SHEET **7**

Device types 01 and 03

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	N/A	H	L	NA	Transmit mode: Transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	N/A	H	H	NA	
L	H	X	X	L	ODD	NA	NA	N/A	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	N/A	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: Transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: Transmits data from T port to R port passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to to transmit mode.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

FIGURE 2. Truth tables.

Error flag output

Device types 01, 02, and 03

Inputs		Internal to device	Outputs pre-state	Output	Function
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	Sample (1's capture)
L	H	X	L	L	
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Device type 04

Inputs		Internal to device	Outputs pre-state	Output	Function
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	↑	H	H	H	Sample (1's capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

NOTE: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

FIGURE 2. Truth tables - Continued.

Device type 02

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit mode: Transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: Transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	*	Receive mode: Transmits data from T port to R port passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	*	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

H = High
L = Low
X = Don't care or irrelevant
Z = High impedance
NA = Not applicable
* = Store the state of the last receive cycle
ODD = Odd number
EVEN = Even number
i = 0, 1, 2, 3, 4, 5, 6, 7

FIGURE 2. Truth tables - Continued.

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: Transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: Transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = High
L = Low
↑ = Low-to-high transition
X = Don't care or irrelevant

Z = High impedance
NA = Not applicable
* = Store the state of the last receive cycle

ODD = Odd number
EVEN = Even number
i = 0, 1, 2, 3, 4, 5, 6, 7

FIGURE 2. Truth tables - Continued.

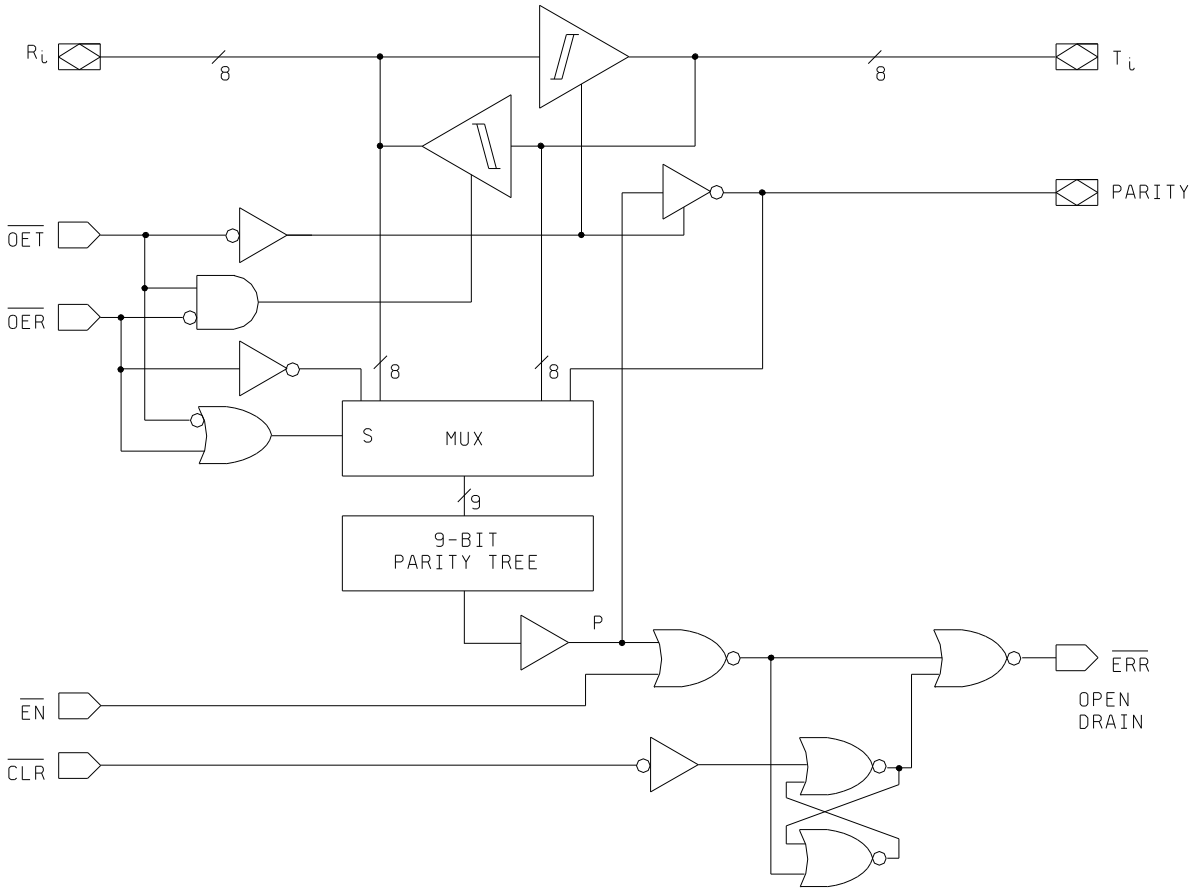


FIGURE 3. Logic diagram.

Device type 02

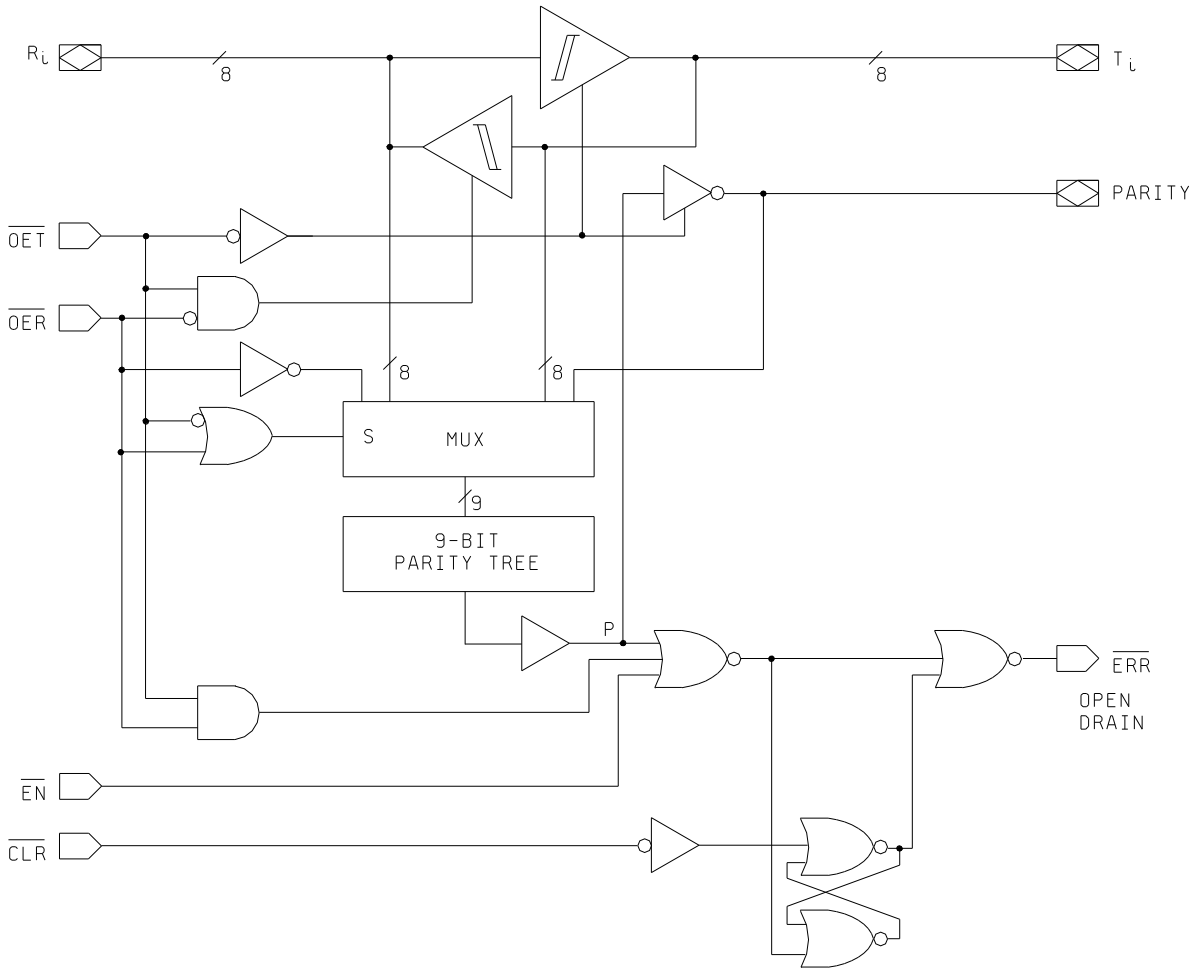


FIGURE 3. Logic diagram - Continued.

Device type 04

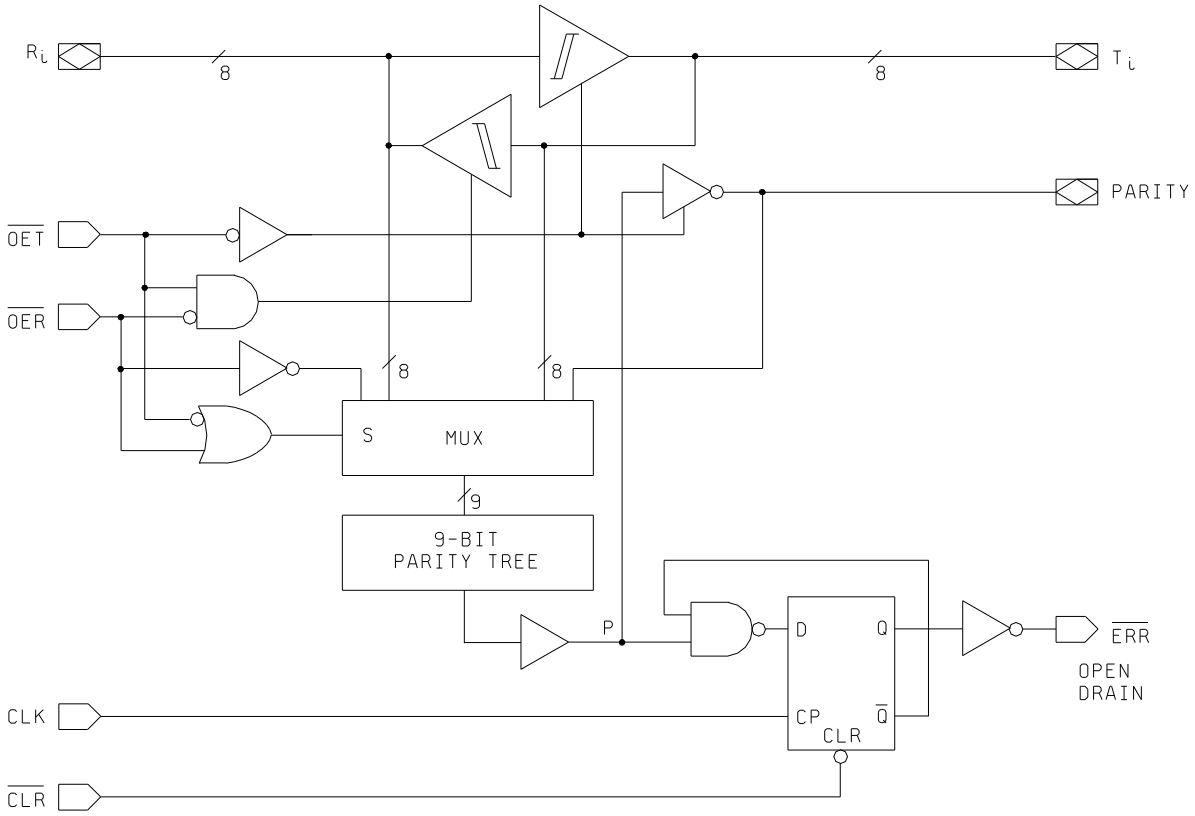
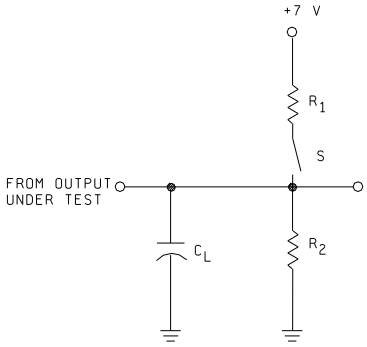
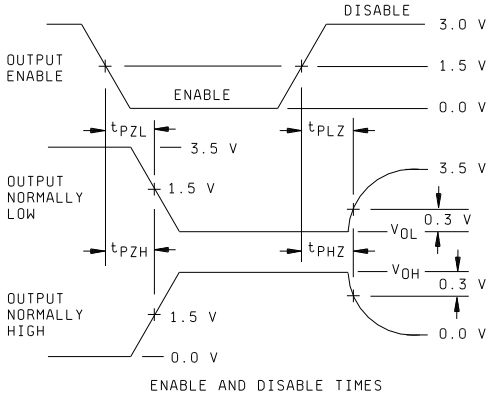


FIGURE 3. Logic diagram - Continued.

Load circuit for three-state outputs





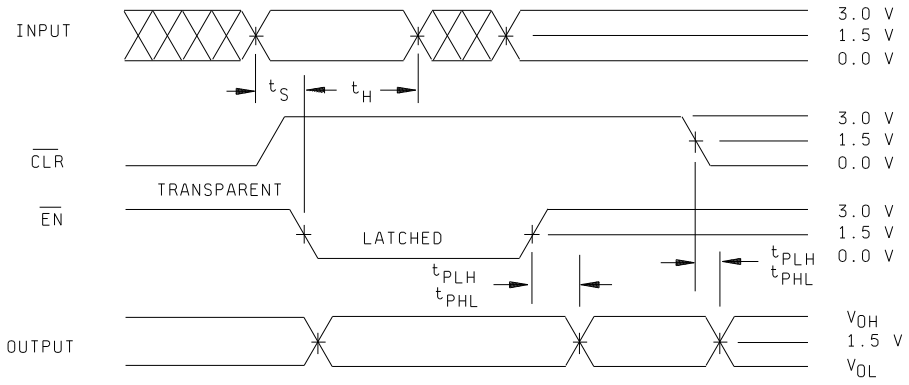
ENABLE AND DISABLE TIMES

Parameter	S position
t_{PLH}	Open
t_{PHL}	Open
t_{PLH} (Open drain output)	Closed
t_{PHL} (Open drain output)	Closed
t_{PHZ}	Open
t_{PZH}	Open
t_{PLZ}	Closed
t_{PZL}	Closed

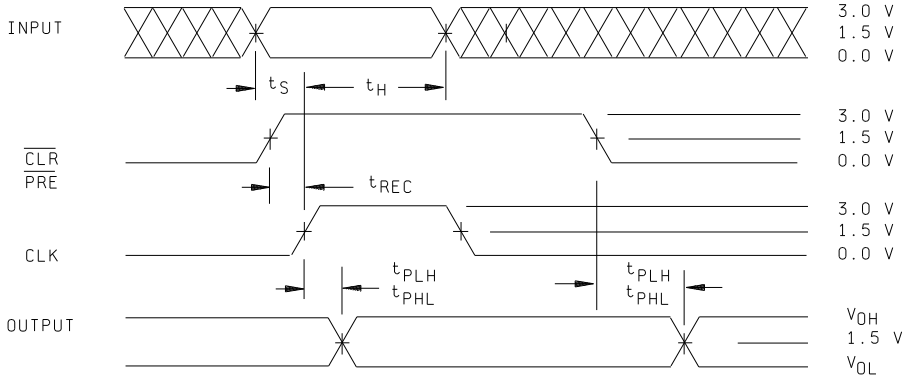
NOTE: Switch is closed for tests on open drain outputs.

Switch positions for parameter testing

FIGURE 4. Switching circuits and waveforms.



Device 04



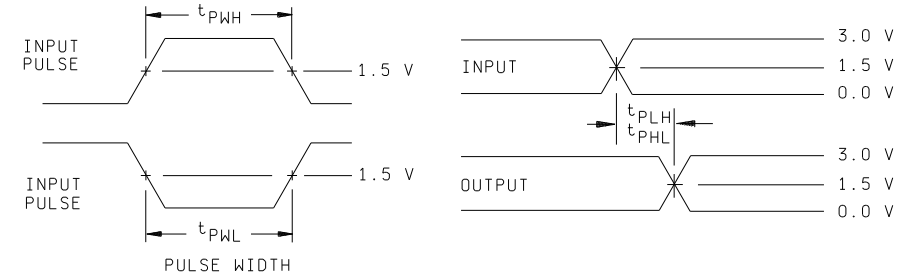


FIGURE 4. Switching circuits and waveforms - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall consist of verification of the truth table.

d. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for initial characterization and after any process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE:

Approved sources of supply for SMD 5962-88573 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8857301LX	34335	AM29C853/BLA
5962-8857301KX	34335	AM29C853/BKA
5962-88573013X	34335	AM29C853/B3A
5962-8857302LX 2/	34335	AM29C855/BLA
5962-8857302KX 2/	34335	AM29C855/BKA
5962-88573023X 2/	34335	AM29C855/B3A
5962-8857303LX	34335	AM29C853A/BLA
5962-8857303KX	34335	AM29C853A/BKA
5962-88573033X	34335	AM29C853A/B3A
5962-8857304LX	34335	AM29C833A/BLA
5962-8857304KX	34335	AM29C833A/BKA
5962-88573043X	34335	AM29C833A/B3A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088